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PROCESS AND SYSTEM EVALUATING DETERMINISTIC BEHAVIOR OF A PACKET SWITCHING NETWORK

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] The present patent document is a continuation of U.S. application serial No. 10/288,025 filed on November 4, 2002, and claims priority to French patent application FR 01 14261 filed on November 5, 2001, the entire contents of each of which are hereby incorporated herein by reference.

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

[0002] This invention relates to a process and system for evaluating the deterministic behavior of a packet switching network, particularly in avionics.

DISCUSSION OF THE BACKGROUND

[0003] The process and system described in documents according to prior art, references [1], [2] and [3] at the end of this description, are based on statistical considerations adapted to land telecommunication networks, but which are not easily adapted for an aircraft.

[0004] The purpose of this invention is to evaluate that a packet switching network actually has a deterministic behavior, particularly in avionics.

SUMMARY OF THE INVENTION

[0005] The invention proposes a process and system for evaluating the deterministic behavior of a packet switching network including subscriber stations connected to each other through at least one switch, this behavior being said to be deterministic in the sense that any packet sent on the network from a source subscriber station reaches the destination subscriber station(s) within a duration that is limited in time. The process and system determine for each output port from each switch on the network if the following relation is satisfied:

i number of virtual links passing through the buffer

$$\left[1 + \text{int}\left(\frac{(Jitter\ \ In)_i + \max Latency}{BAGi}\right)\right] *$$

(max frame duration) ≤ latency

[0006] in which:

[0007] the max latency value is the maximum residence time in the output buffer of a switch, this value may be different for each switch in the network.

[0008] BAGi is the minimum time between two consecutive frames belonging to a vertical link i, before they are transmitted on the physical support.

[0009] (Jitter In)i is the Jitter associated with a virtual link i that represents the time interval between the theoretical instant at which a frame is transmitted, and its effective transmission which may be before or after the theoretical instant.

[0010] (max frame duration) i is the duration of the longest frame on the virtual link i.

[0011] In another embodiment, virtual links are added one by one, checking that the behavior of the entire network actually remains deterministic after each addition of a virtual link.

[0012] In avionics, the invention solves a security requirement that is of prime importance for the transport of information on an aircraft, called "determinism". It is essential that data is actually received within a maximum time after being sent to a destination, and this maximum time must be known.

[0013] The process and system according to the invention has the advantage that it is extremely easy to use (only one equation for each output port). It is analytic and requires only very little information about the network characteristics (maximum latency per switch, BAG and subscriber jitter).

[0014] The invention is useful for all packet switching networks for which a particularly service quality is required in terms of information routing guarantee, for example "Fast Ethernet", ATM ("Asynchronous Transfer Mode"), etc.

[0015] Preferred applications are aeronautics (civil and military), space, marine and nuclear.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] A more complete appreciation of the present invention and many of the attendant advantages thereof will be readily obtained as the same becomes better understood by reference to the following detailed description when considered in connection with the accompanying drawings, wherein:

[0017] FIG. 1 illustrates a model of an end system.

[0018] FIG. 2 illustrates jitter for a regular flow.

[0019] FIGS. 3A to 3C illustrate the position of frames within their jitter window.

[0020] FIG. 4 illustrates a switch model.

[0021] FIGS. 5A to 5G illustrate the position of the sliding window for an example (BAG, Jitter In).

[0022] FIG. 6 illustrates an example topology.

[0023] FIG. 7 illustrates the number of virtual links for the topology illustrated in FIG. 6.

[0024] FIGS. 8A and 8B illustrate an example aggregation of virtual links.

[0025] FIG. 9 illustrates an example embodiment in avionics.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0026] The invention relates to a process and system for checking the deterministic behavior of a packet switching network. This process and system guarantee that such a network has a deterministic behavior, in the sense that any packet sent on the network from a source node reaches the destination node(s) within a duration that is limited in time. Such a process is applicable to all networks based on packet switching or frame switching or cell switching. It makes it possible to be certain that the configuration of a network through switch routing tables and the frame flows passing through the switches, is conforming with a deterministic behavior.

[0027] In the remainder of the description, an end system refers to a node in a network capable of generating and receiving frames but which is not an intermediate node (switch, router, gateway, etc.) that is designed to route the frames in the network. When an intermediate node is the source of a flow of frames addressed to one or several end systems, it behaves like an end system.

[0028] A virtual link (VL) is a logical connection between a source end system and one or several destination end systems.

[0029] Each virtual link has a specific value called the Bandwidth Allocation Gap (BAG), which has one second as its unit, which represents the minimum time separating two consecutive frames belonging to the virtual link in question and before they are sent on the physical support.

[0030] A model of an end system is shown in FIG. 1. The input is irregular flows of packets 10 from applications (asynchronous flows between virtual links VL1, VL2, VL3). Packet flows are then regulated by means of regulators 11 each corresponding to a virtual link in

order to separate packets in BAG gaps. A multiplexer 12 then outputs a flow of frames 13 on the physical support 14.

[0031] The jitter associated with a virtual link represents the time interval between the theoretical moment at which a frame is transmitted (relative to the BAG) and when it is actually transmitted, that may be before or after the theoretical instant.

[0032] The flow of frames in a virtual link is entirely characterized by the (BAG, max Jitter) pair, in which max jitter is the maximum value of the instantaneous jitter that can be obtained for this virtual link.

[0033] The term jitter refers to the max jitter throughout the remainder of this document.

[0034] For a virtual link for which the flow is maximum (always one frame to be sent) and regular, there is one frame 20 precisely at each BAG gap as shown in FIG. 2. The jitter associated with this virtual link is zero.

[0035] In the general case, the start of the frame transmission may occur at any position within the jitter gap. If the frame 1 is delayed as it passes through the switch, and then a few instants later frame 2 in the same virtual link is only slightly delayed, the BAG value is no longer respected. Therefore the flow of frames in the same virtual link has a certain jitter relative to the BAG value.

[0036] The three cases illustrated in FIGS. 3A, 3B and 3C show the position of the frames within their jitter window.

[0037] FIG. 3A illustrates the case in which Jitter<BAG.

[0038] FIG. 3B illustrates the case in which Jitter=BAG. When Jitter=BAG, there is a purely theoretical possibility that a frame will be overlapped by another frame that is very early. Since the transmission order is guaranteed, this possibility is prohibited since a frame transmitted after another frame cannot overlap or be later than the other frame. Therefore, the two frames appear side by side (called frame bursts).

[0039] FIG. 3C illustrates the case in which Jitter>BAG. Jitters mutually overlap and frame 2 is transmitted immediately after frame 1. There is a burst.

[0040] The jitter associated with each virtual link at the output from an end system, which is equal to Jitter ES, is equal to the contention that takes place at the output from the end system in which several regulated flows want to access the same FIFO (First In-First Out) output register. Its value depends on a number of variables including the number of virtual links connected to the end system.

[0041] Thus, all virtual links output from an end system have the (BAG, Jitter ES) characteristic.

[0042] A switch model is illustrated in FIG. 4, with input buffers 30, a demultiplexer 31, a multiplexer 32 and output buffers 33.

[0043] According to this model, it can be seen that there will be "more or less" contention for access to the output ports, depending on the configuration of the switch (forwarding table) and the flow characteristics of virtual links arriving in the input ports. The effect of this contention is to generate delays and therefore pollution on the flow characteristic of each virtual link at the output ports.

[0044] Depending on the instantaneous load of a switch, a frame may either remain in the switch for a minimum time (minimum latency) or remain in it for a maximum time (maximum latency of the switch) or remain in it for any intermediate duration.

[0045] If the flow characteristic of a virtual link input into the switch is (BAG, Jitter In), then the magnifying disturbance generated by the switch will introduce a new characteristic for the flow in the same virtual link at the output from the switch: (BAG, Jitter Out) where Jitter Out=Jitter In+max latency.

[0046] In order to demonstrate determinism, it is necessary to size the output buffers such that no frames are lost, using a given switch configuration as a starting point together with the characteristics of the virtual links passing through the switch.

[0047] For a given virtual link with the (BAG, Jitter In) characteristic, the formula giving the maximum number of frames associated with this virtual link that can take place during a sliding window FG with a duration of T seconds, is:

$$N=1+\text{int}(\text{Jitter In}+T/\text{BAG})\text{unit=frames per sliding window T}$$

where the function int(x) returns the integer part of x (to round to the next lowest integer)

$$\text{for x from } [0, 1[, \text{ int}(x)=0$$
$$\text{for x from } [1, 2[, \text{ int}(x)=1$$

[0048] For example, if the reference interval T=1 ms is used, this formula implies:

[0049] BAG+2 ms/Jitter In=0.5 ms=>1+int((0, 5+1)/2)=1 frame max/ms (see FIG. 5A).

[0050] BAG=2 ms/Jitter In=1 ms=>1+int((1+1)/2)=2 frames max/ms (see FIG. 5B). In this case, two frame transmission events may take place during 1 ms and therefore two complete

frames may be located in the buffer (we might thought that there would only be one frame during 1 ms).

[0051] BAG=2 ms/Jitter In=1.5 ms=>1+int((1.5+1)/2)=2 max frame 2 frames max/ms (see FIG. 5C)

[0052] BAG=2 ms/Jitter In=2 ms=>1+int((2+1)/2=2 frames max/ms (see FIG. 5D)

[0053] BAG=2 ms/Jitter In=2.5 ms=>1+int((2.5+1)/2=2 frames max/ms (see FIG. 5E)

[0054] BAG=2 ms/Jitter In=3 ms=>1+int((3+1)/2)=3 frames max/ms (see FIG. 5F)

[0055] BAG=2 ms/Jitter In=4 ms=>1+int((4+1)/2)=3 frames max/ms (see FIG. 5G).

[0056] To prevent congestion of a switch output buffer so that frames will never be lost, a switch is necessary for each output port and the following relation must be satisfied for all switches in the network.

$$\sum_{\substack{i \text{ number of virtual links} \\ \text{passing through the buffer}}} \left[1 + \text{int}\left(\frac{(Jitter\ \ In)_i + \max Latency}{BAGi}\right)\right] * (\text{max frame duration}) \leq latency$$

[0057] The max latency value is the maximum residence time in a switch output buffer and it may be different for each switch in the network. The left part represents the duration of all frames of all virtual links that can reside in a switch output buffer and using the max latency time as the sliding window. If this relation is satisfied, there is no congestion and the flow characteristic of a virtual link is transformed from (BAG, Jitter In) to (BAG, Jitter Out=Jitter In+max latency). In other words, the switch configuration agrees with the performances of the switch (max latency).

Application to a Simple Network

[0058] FIG. 6 illustrates a topology. It is considered that each end system ES1, ES2, ES3 or ES4 has virtual links that lead to all other end systems ("broadcast" case). Each end system has an identical number Ni of virtual links with characteristics BAG=2 ms and Jitter ES=0.5 ms.

[0059] FIG. 7 shows a diagram representing the number Ni of virtual links on each simple link.

[0060] The calculations are as follows:

[0061] On the two central links:

[0062] N1[1+int((0.5+1)/2]*15.52+N2[1+int((0.5+1)/2]*15.52<1000 μs

[0063] (N1+N2)*15.52<1000 μs

[0064] Similarly on the other link:

[0065] (N3+N4)*15.52<1000 μs

[0066] The formula for the uplink to ES1 is:

[0067] N2[1+int((0,5+1)/2]*15.52+N3[1+int((1.5+1)/2)]*15.52*N4[1+int((1.5+1)/2]*15.52<1000 μs

[0068] N2*15.52+2*(N3+N4)15.52<1000 μs

[0069] The other uplinks are similar, with appropriate end systems.

[0070] We also have the equation: N1=N2=N3=N4, in which 5.N1.15.52<1000 μs.

[0071] N1=N2=N3=N4=12 virtual links.

[0072] Therefore the number of virtual links on an uplink to an end system is 3*12=36 virtual links. A frame size of 174 bytes gives a physical flow for a virtual link with BAG=2 ms equal to 1000/2*(174+20)8*=776 000 bit/s. This gives 36 virtual links corresponding to a physical flow of 36*776 000=27.936 Mbits/s.

[0073] It can be seen that most of the disturbance generated by a chosen switch has divided the theoretical physical flow that would have occurred on the link (100 Mbits/s) by more than 3.

[0074] It is particularly important to note that a virtual link with a BAG equal to 128 ms is as expensive for the network, for example as a virtual link with a BAG equal to 4 ms (if the jitter is less than 2). This is due to the 1 term in the formula 1+int(Jitter+T)/BAG).

[0075] In another advantageous embodiment of the process according to the invention, an incremental approach is used in which the virtual links are added one by one, checking that the behavior of the complete network remains deterministic after adding a virtual link.

Aggregation of Virtual Links

[0076] One possible optimization to overcome the disadvantage described above is to aggregate several virtual links to form a single super-virtual link that will be used as a basis in the non-congestion calculation.

[0077] Aggregation refers to the fact that several virtual links with a large BAG can be re-regulated with a lower BAG value, such that the low speed virtual links behave like a single higher speed virtual link.

[0078] FIG. 8A illustrates an example. There are four virtual links VL1, VL2, VL3 and VL4 with BAG=2 ms and three virtual links VL5, VL6 and VL7 with BAG=8 ms.

[0079] The first 40 of the seven regulators 41 acts as a smoother for the virtual links with BAG=8 ms. Since the 0.5 ms jitter is guaranteed for the output flow from this regulator, the virtual links with BAG=8 ms also have the same jitter value. On the other end, it is clear that this model generates more latency for virtual links with BAG=8 ms.

[0080] To make smoothing possible, the non-saturation condition of the first regulator needs to be satisfied.

[0081] Number of virtual links to be smoothed x BAG smoothing $\leq$ min ($BAG_{virtual\ link}$).

[0082] This aggregation of virtual links does not cause any loss of segregation. With these virtual links, a packet flow illustrated in FIG. 8B can be achieved with the indicated numbers being the numbers for the virtual links.

[0083] Therefore, with the process according to the invention, it is quite possible to have a large number of virtual links while keeping the mentioned non-congestion property.

[0084] FIG. 9 illustrates an example embodiment for use of the process according to the invention in avionics. In this example, a first switch 50 is connected firstly to a first graphic screen 51 (flight parameters) and to a second graphic screen (flight and maintenance parameters), and secondly to a second switch 53 itself connected to a flight parameters generator 54 and an aircraft maintenance computer 55.

[0085] Obviously, numerous modifications and variations of the present invention are possible in light of the above teachings. It is therefore to be understood that within the scope of the appended claims, the invention may be practiced otherwise than as specifically described herein.

REFERENCES

[0086] [1] "Queuing delays in rate controlled networks" by Barnejea and S. Keshav (Proceedings of IEEE INFOCOM'93, pages 547-556, San Francisco, Calif., April 1993).

[0087] [2] "A calculus for network delay" by R. Cruz (Part 1 Network elements in isolation. IEEE Transaction of Information Theory, 37(1), pages 121-141, 1991).

[0088] [3] "A calculus for network delay" by R. Cruz (Part II: Network analysis. IEEE Transaction of Information Theory, 37(1), pages 121-141, 1991).